Course Contents for Bridge Course on "Digital Circuit Design using VHDL"

(1st July, 2019-10th July, 2019)

Date	Topic	Faculty	Timings
01-07-2019	**Session 1**: VHDL Introduction	Er. Harleen Kaur	9 am-11 am
	Session 2: Software Overview	Er. Harleen Kaur	11:30am-1:30pm
02-07-2019	**Session 1:** VHDL Tutorial	Er. Kirandeep Kaur	9 am-11 am
	Session 2: Practical Session on design of basic gates	Er. Kirandeep Kaur	11:30am-1:30pm
03-07-2019	**Session 1:** Identifier, Data Objects & Data Types	Er. Harleen Kaur	9 am-11 am
	Session 2: Practical Session on combinational circuits	Er. Harleen Kaur	11:30am-1:30pm
04-07-2019	**Session 1:** Operators - Behavioral Modeling-Process, variable and Signal Assignment statement, Wait statement, IF statement	Er. Gurinder Singh	9 am-11 am
	Session 2: Practical Session on Operators	Er. Gurinder Singh	11:30am-1:30pm
05-07-2019	**Session 1:** Behavioral Modeling: CASE statement, NULL statement, LOOP, EXIT, NEXT statement, REPORT statement	Er. Kirandeep Kaur	9 am-11 am
	Session 2: Practical Session on Behavioral modeling	Er. Kirandeep Kaur	11:30am-1:30pm
08-07-2019	**Session 1:** Data Flow Modeling-concurrent signal assignment, Concurrent vs Signal, Delta Delay, Conditional Assignment statement, Select statement, unaffected, block.	Er. Shyna Kalra	9 am-11 am
	Session 2: Practical Session on Data flow modeling	Er. Shyna Kalra	11:30am-1:30pm
09-07-2019	**Session 1**: Structure Modeling	Er. Shyna Kalra	9 am-11 am
	Session 2: Practical Session on Structure Modeling	Er. Shyna Kalra	11:30am-1:30pm

07-2019	**Session 1:** Generics configuration, Subprogram and overloading, Library and packages	Er. Kirandeep Kaur	9 am-11 am
	Session 2: Miscellaneous programs using various architecture styles	Er. Kirandeep Kaur	11:30am-1:30pm

Practical Session includes design of various digitals circuits using VHDL:

1. Design of logic gates: AND, OR, NOT, NAND, NOR, XOR and XNOR.
2. Design of adder and subtractor.
3. Design of 8:1 MUX and 1:4 DEMUX using various styles of modeling.
4. Design of 2:4 and 3:8 decoder using various styles of modeling.
5. Design of code converter various styles of modeling.
6. Design of BCD to 7-segment display.
7. Design of 2-bit comparator using if-else statement.
8. Design of D flip-flop, SR flip-flop.
9. To find largest number out of given numbers.
10. Design 9-bit parity generator.

Venue: Microprocessor Lab

Navneet Kaur